What is claimed is:

1. An address sub-sampling apparatus, comprising:

a counting unit that generates a binary address of N bits, N being a natural number larger than 2; and

an address conversion unit that sub-samples the binary address of N bits to output a sub-sampled address having first, second and third bit groups, wherein the sub-sampled address is arranged in order of the third, the first and the second bit groups from the MSB (Most Significant Bit), the first bit group, which is a combination of digits in the sub-sampled address corresponding to the number of addresses to be skipped, being set as "0", the second bit group, which includes the LSB (Least Significant Bit) corresponding to bits of the binary address, and the third bit group, which includes the MSB being set to shift address subtracted by the number of bits in the first bit group from the MSB in the binary address.

2. The apparatus of claim 1, further comprising a multiplexing unit that selects one of a plurality of predetermined sub-sampling modes provided from the binary address of N bits, wherein the address conversion unit performs the sub-sampling operation in accordance with the selected sub-sampling mode.

3. The apparatus of claim 1, wherein the number of the plurality of predetermined sub-sampling modes is 2^N-1.

4. The apparatus of claim 1, wherein the number of the addresses to be skipped and the number of addresses to be outputted are both even numbers.

5. An image sensor of line scanning manner, comprising:

a first counting unit that generates a first binary address of X bits in synchronization with a preset data clock signal, X being a natural number larger than 2;

a first address conversion unit that sub-samples the first binary address of X bits to provide a first sub-sampled address having first, second and third bit groups;

a second counting unit that generates a second binary address of Y bits in synchronization with a preset line clock signal, Y being a natural number larger than 2; and

a second address conversion unit that sub-samples the second binary address of Y bits to output a second sub-sampled address having first, second and third bit groups,

wherein each of the first and the second sub-sampled addresses is arranged in order of the third, the first and the second bit groups from the MSB (Most Significant Bit), the first bit group, which is a combination of digits in the sub-sampled address corresponding to the number of addresses to be skipped, being set as "0", the second bit group, which includes the LSB (Least Significant Bit) corresponding to bits of the binary address, and the third bit group, which includes the MSB being set to shift address subtracted by the number of bits in the first bit group from the MSB in the binary address.

6. The image sensor of claim 5, wherein the first address conversion unit generates a sub-sampled column address, and the second address conversion unit generates a sub-sampled row address.

7. The image sensor of claim 6, further comprising:

a first multiplexing unit that selects a first sub-sampling mode from a first plurality of predetermined sub-sampling modes provided from the first binary address of X bits; and

a second multiplexing unit that selects a second sub-sampling mode from a second plurality of predetermined sub-sampling modes provided from the second binary address of Y bits,

wherein each of the first and the second address conversion units performs sub-sampling operations in accordance with the selected first and second sub-sampling modes, respectively.

8. The image sensor of claim 7, wherein the number of the first plurality of predetermined sub-sampling modes is 2^X-1, and the number of the second plurality of predetermined sub-sampling modes is 2^Y-1.

9. The image sensor of claim 5, wherein the number of the addresses to be skipped and the number of addresses to be outputted are both even numbers.

10. The image sensor of claim 5, wherein the preset line clock signal has a time period that is obtained by adding a time interval between the lines to a value that is calculated by multiplying a width of a column of a pixel arrangement device by the data clock signal.

11. An address sub-sampling method, comprising:

generating a binary address of N bits, N being a natural number larger than 2; and

sub-sampling the binary address of N bits to output a sub-sampled address that is provided in such a way that third, first, and second bit groups of the sub-sampled addresses are arranged in sequence from the MSB (Most Significant Bit), the first bit group, which is a combination of digits in the sub-sampled address corresponding to the number of addresses to be skipped, being set as "0", the second bit group, which includes the LSB (Least Significant Bit) corresponding to bits of the binary address, and the third bit group, which includes the MSB being set to shift address subtracted by the number of bits in the first bit group from the MSB in the binary address.

12. A sub-sampling method for use in an image sensor, comprising:

generating a first binary address of X bits in synchronization with a preset data clock signal, and generating a second binary address of Y bits in synchronization with a preset line clock signal, both X and Y being natural numbers larger than 2; and

sub-sampling the first and the second binary addresses to output first and second sub-sampled addresses that are provided in such a way that third, first, and second bit groups of each of the first and the second sub-sampled addresses are arranged in sequence from the MSB (Most Significant Bit), the first bit group, which is a combination of digits in the sub-sampled address corresponding to the number of addresses to be skipped, being set as "0", the second bit group, which includes the LSB (Least Significant Bit) corresponding to bits of the binary address, and the third bit group, which includes the MSB being set to shift address subtracted by the number of bits in the first bit group from the MSB in the binary address.

13. The method of claim 12, wherein the first sub-sampled address is a column address and the second sub-sampled address is a row address.

14. The method of claim 12, wherein the preset line clock signal has a time period that is obtained by adding a time interval between the lines to a value that is calculated by multiplying a width of a column of a pixel arrangement device by the data clock signal.